In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1   1.   (Currently Amended) A method of operating a digital
2 system having a processor and associated translation lookaside
3 buffer (TLB), comprising the steps of:
4   executing a plurality of program tasks within the processor;
5   initiating a plurality of memory access requests in response
6 to the plurality of program tasks;
7   caching a plurality of translated memory addresses in the TLB
8 responsive to the plurality of memory access requests;
9   incorporating a task identification value with each translated
10 memory address to indicate which of the plurality of program tasks
11 requested the respective translated memory address;
12   incorporating a shared indicator with each translated memory
13 address to indicate when a translated memory address is shared by
14 more than one of the plurality of program tasks; and
15   invalidating a portion of the plurality of translated memory
16 address in the TLB in a manner that is qualified by the shared
17 indicator in response to an invalidate TLB entry command issued
18 from the processor ~~and not changing data in any other memory~~.

1   2.   (Previously Amended) The method according to Claim 1,
2 wherein:
3   said invalidate TLB entry command comprises an invalidate
4 shared TLB entry command; and
5   the step of invalidating in response to an invalidate shared
6 TLB entry command comprises invalidating a translated memory
7 address in the TLB only if the corresponding shared indicator
8 indicates the translated memory address is shared by more than one
9 of the plurality of program tasks.

-2-

1   3.   (Previously Amended) The method according to Claim 1,

2 wherein:

3   said invalidate TLB entry command comprises an invalidate task

4 TLB entry except shared command, said invalidate task TLB entry

5 except shared command identifying one of the plurality of program

6 tasks; and

7   the step of invalidating in response to an invalidate task TLB

8 except shared command comprises invalidating a translated memory

9 address in the TLB only if the corresponding task identification

10 value indicates the program task identified by said invalidate task

11 TLB entry except shared command and the corresponding shared

12 indicator indicates the translated memory address is not shared by

13 more than one of the plurality of program tasks.

Claims 4 to 13.   (Canceled)

1   14.   (Currently Amended) A digital system having a translation

2 lookaside buffer (TLB), the TLB comprising:

3   storage circuitry with a plurality of entry locations for

4 holding translated values, wherein each of the plurality of entry

5 locations includes a first field for a translated value and a

6 second field for an associated shared indicator;

7   a set of inputs for receiving a translation request;

8   a set of outputs for providing a translated value selected

9 from the plurality of entry locations; and

10   control circuitry connected to the storage circuitry, wherein

11 the control circuitry is responsive to an invalidate TLB entry

12 command to invalidate entries within said storage circuitry

13 qualified by the shared indicator field ~~not change data in any~~

14 ~~other memory~~.

- 3 -

1   15. (Previously Amended) The digital system of Claim 14,
2   wherein the digital system further comprises a second level TLB
3   connected to the TLB, the second level TLB comprising:
4   second level storage circuitry with a plurality of entry
5   locations for holding translated values, wherein each of the
6   plurality of entry locations includes a first field for a
7   translated value and a second field for an associated shared
8   indicator; and
9   wherein the control circuitry is connected to the second level
10   storage circuitry, the control circuitry being responsive to an
11   invalidate TLB entry command to invalidate selected ones of the
12   plurality of entry locations in the second storage circuitry
13   qualified by the shared indicator field.

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     Claim 16. (Canceled)

1   17. (Previously Added) The digital system of Claim 14,
2   wherein:
3   said invalidate TLB entry command comprises an invalidate
4   shared TLB entry command; and
5   said control circuitry being responsive to an invalidate
6   shared TLB entry command comprises to invalidate a translated
7   memory address in the storage circuitry only if the corresponding
8   shared indicator indicates the translated memory address is shared
9   by more than one of the plurality of program tasks.

1   18. (Previously Added) The digital system of Claim 14,
2   wherein:
3   said storage circuitry wherein each of the plurality of entry
4   locations includes a third field for a task identification value;
5   said invalidate TLB entry command comprises an invalidate task
6   TLB entry except shared command, said invalidate task TLB entry

— 4 —

7   except shared command identifying one of a plurality of task

8   identification values; and

9   control circuitry being responsive to an invalidate task TLB

10 except shared command to invalidate a translated memory address in

C₁   11 the storage circuitry only if the corresponding task identification

12 value corresponds to said task identification value of said

13 invalidate task TLB entry except shared command and the

14 corresponding shared indicator indicates the translated memory

15 address is not shared.

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